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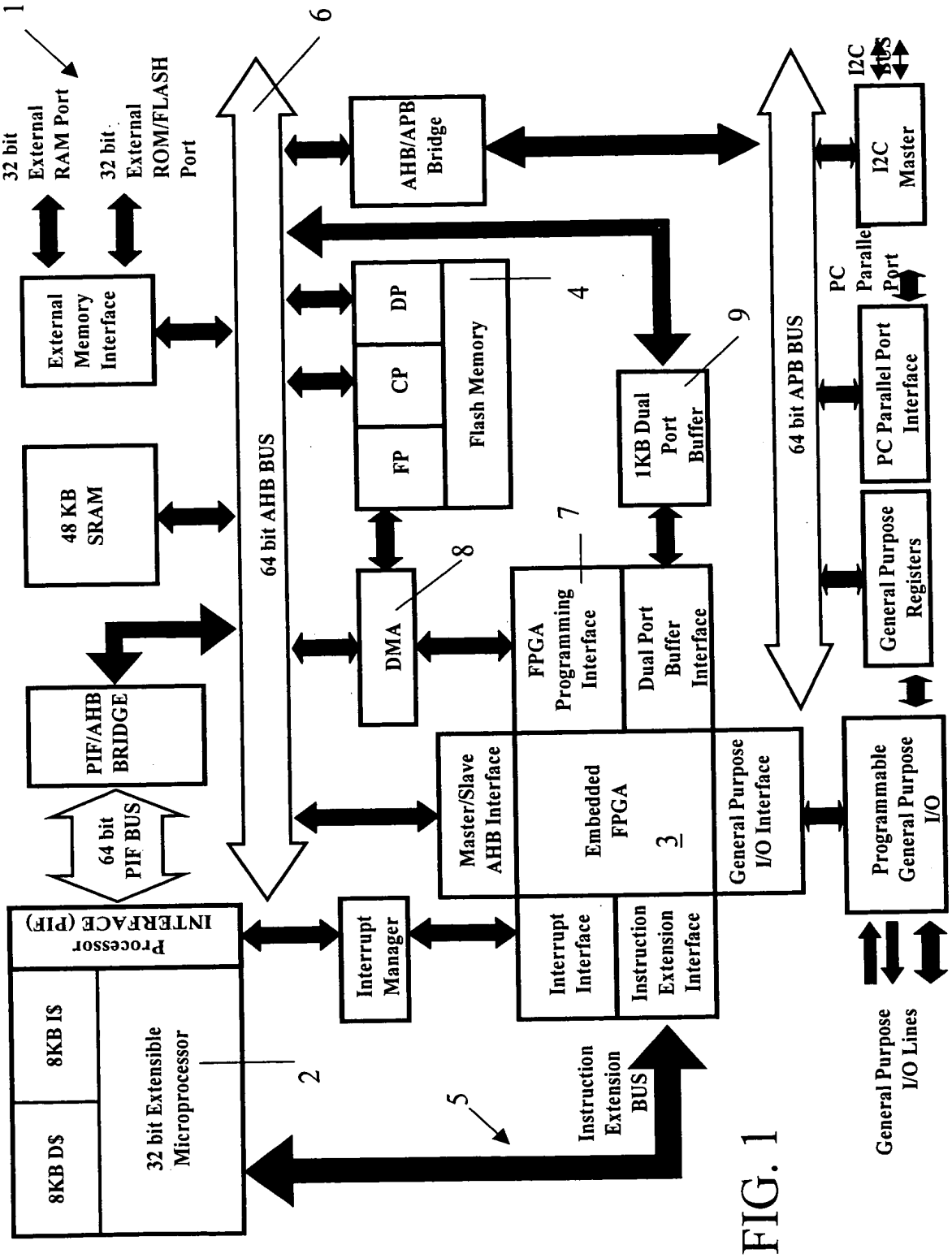
1
32 bit External RAM Port
32 bit External ROM/FLASH Port
External Memory Interface
48 KB SRAM
PIF/AHB BRIDGE
64 bit PIF BUS
Processor INTERFACE (PIF)
8KB D$
8KB I$
32 bit Extensible Microprocessor
2
5
6
64 bit AHB BUS
AHB/APB Bridge
DP
CP
FP
Flash Memory
4
DMA
8
Interrupt Manager
Interrupt Interface
Instruction Extension Interface
Instruction Extension BUS
7
FPGA Programming Interface
Dual Port Buffer Interface
Master/Slave AHB Interface
Embedded FPGA
3
General Purpose I/O Interface
9
1KB Dual Port Buffer
64 bit APB BUS
I2C BUS
I2C Master
PC Parallel Port
PC Parallel Port Interface
General Purpose Registers
Programmable General Purpose I/O
General Purpose I/O Lines

FIG. 1

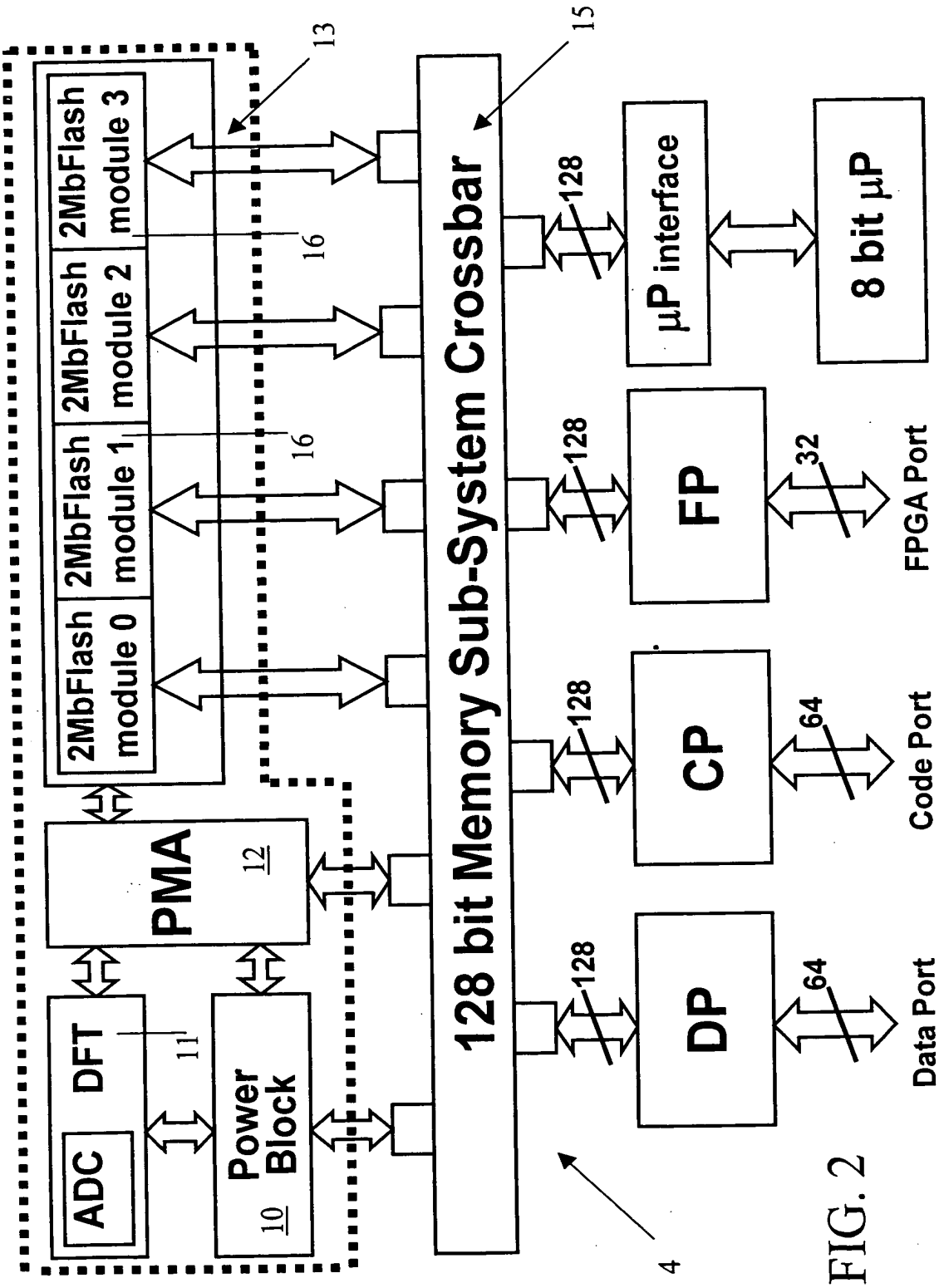
2MbFlash module 3
2MbFlash module 2
2MbFlash module 1
2MbFlash module 0
13
15
16
16
PMA
12
DFT
ADC
11
Power Block
10
128 bit Memory Sub-System Crossbar
128
µP interface
8 bit µP
128
FP
32
FPGA Port
128
CP
64
Code Port
128
DP
64
Data Port
4

FIG. 2

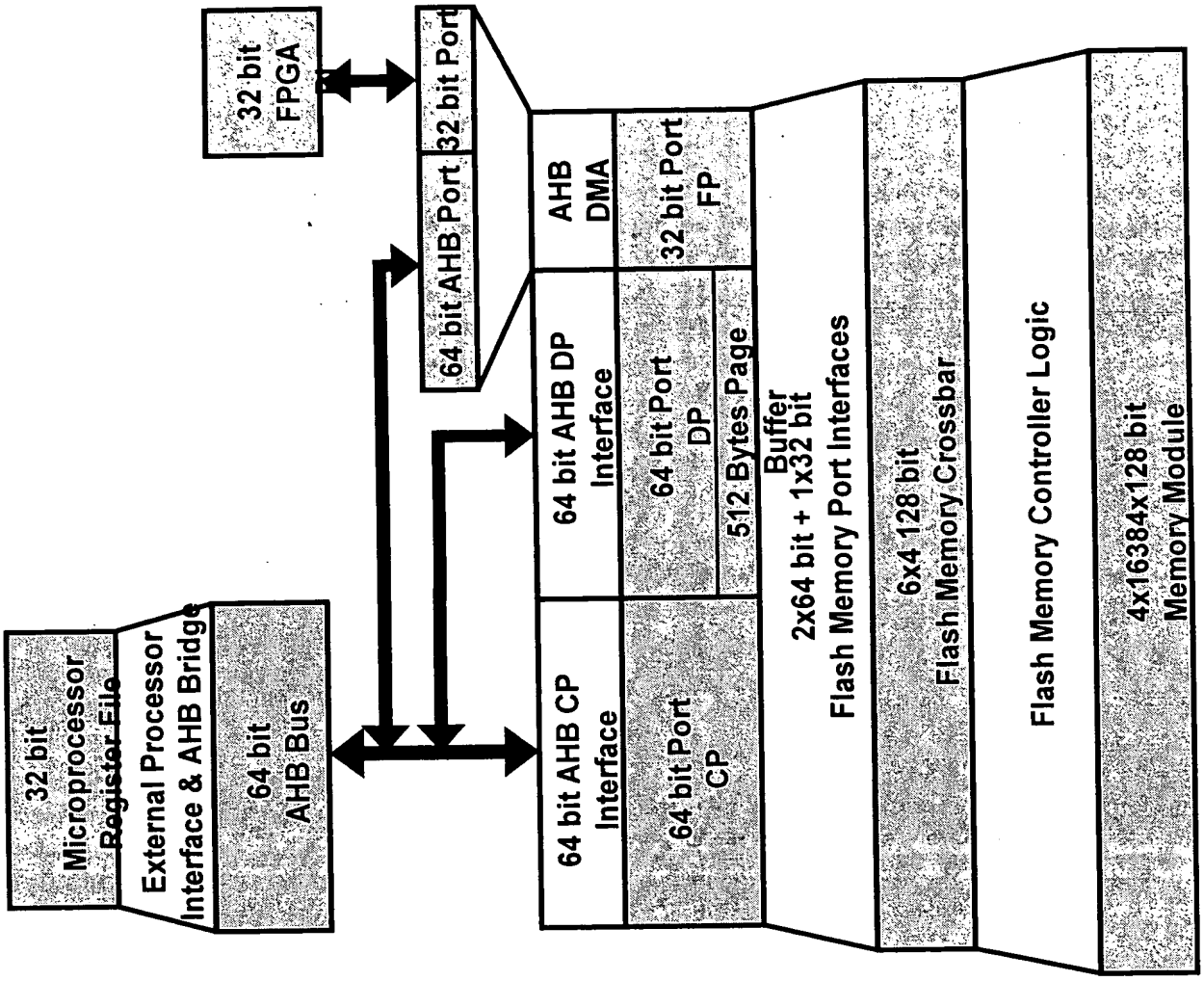
32 bit
Microprocessor
Register File
External Processor
Interface & AHB Bridge
64 bit
AHB Bus
32 bit
FPGA
64 bit AHB Port
32 bit Port
64 bit AHB CP
Interface
64 bit AHB DP
Interface
AHB
DMA
64 bit Port
CP
64 bit Port
DP
512 Bytes Page
Buffer
32 bit Port
FP
2x64 bit + 1x32 bit
Flash Memory Port Interfaces
6x4 128 bit
Flash Memory Crossbar
Flash Memory Controller Logic
4x16384x128 bit
Memory Module

FIG. 3

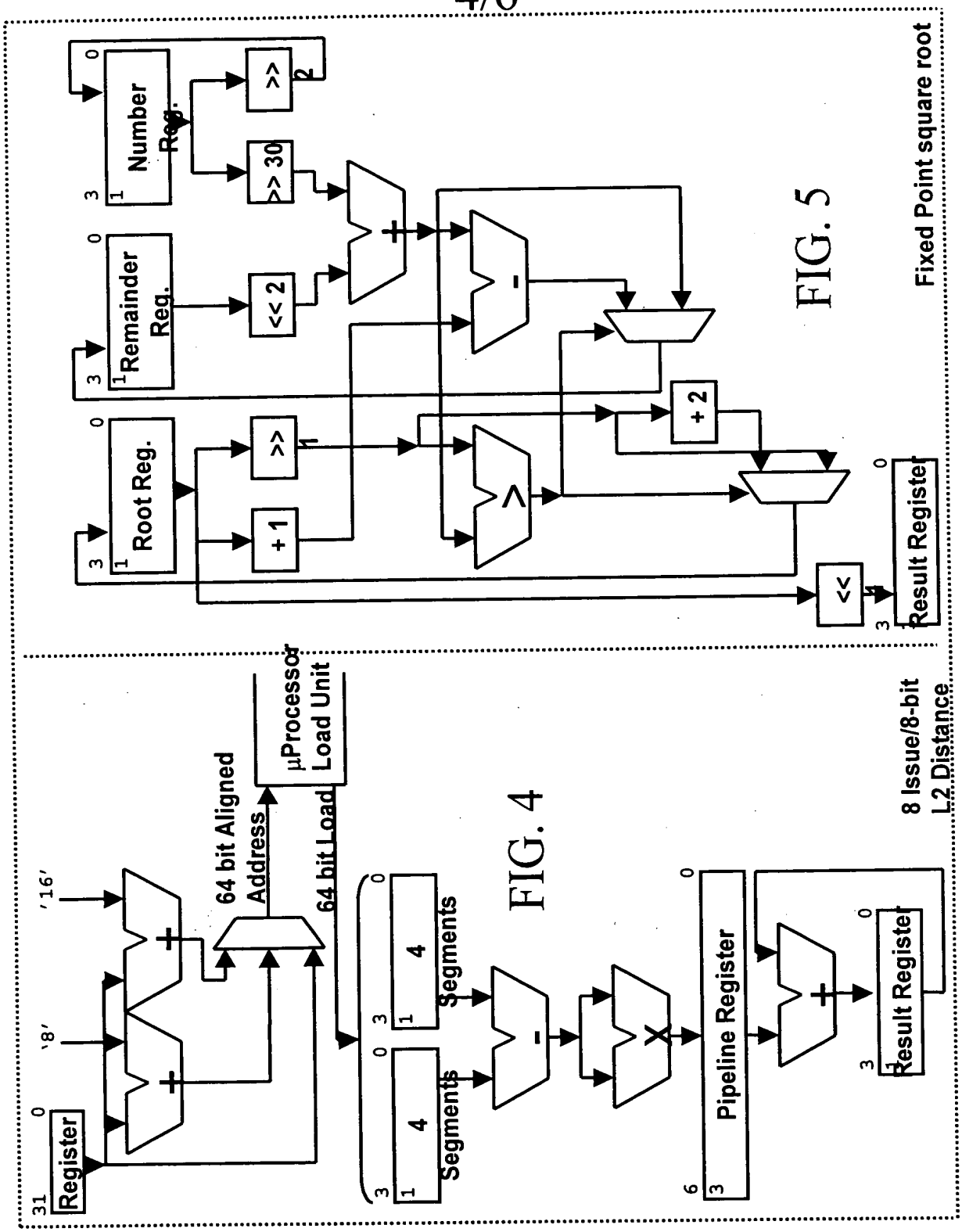
Register
'16'
'8'
64 bit Aligned Address
µProcessor Load Unit
64 bit Load
Segments
Segments
Pipeline Register
Result Register
8 Issue/8-bit L2 Distance
Root Reg.
Remainder Reg.
Number Reg.
+ 1
>>
<< 2
>> 30
>>
+ 2
<<
Result Register
Fixed Point square root

FIG. 4

FIG. 5

Algorithm Stage	*RISC with basic DSP instruction support*	*RISC with Microprocessor Extensions*	*Speed-Up*	*Energy Gain*	*Energy Efficiency Gain (Energy x Delay)*
Bayer filter	58 msec	24.7 msec	x 2.3	x 1.4	x 3.22
Edge detection	4.5 msec	2.5 msec	x 1.8	x 0.95	x 1.71
Face detection	1.5 sec	382 msec	x 4	x 2.9	x 11.6
Face recognition (Twenty face database)	9.15 sec	860 msec	x 10.6	x 9	x 95.4
Totals	**10.7 sec**	**1.26 sec**	**x 8.5**	**x 6.7**	

FIG. 6

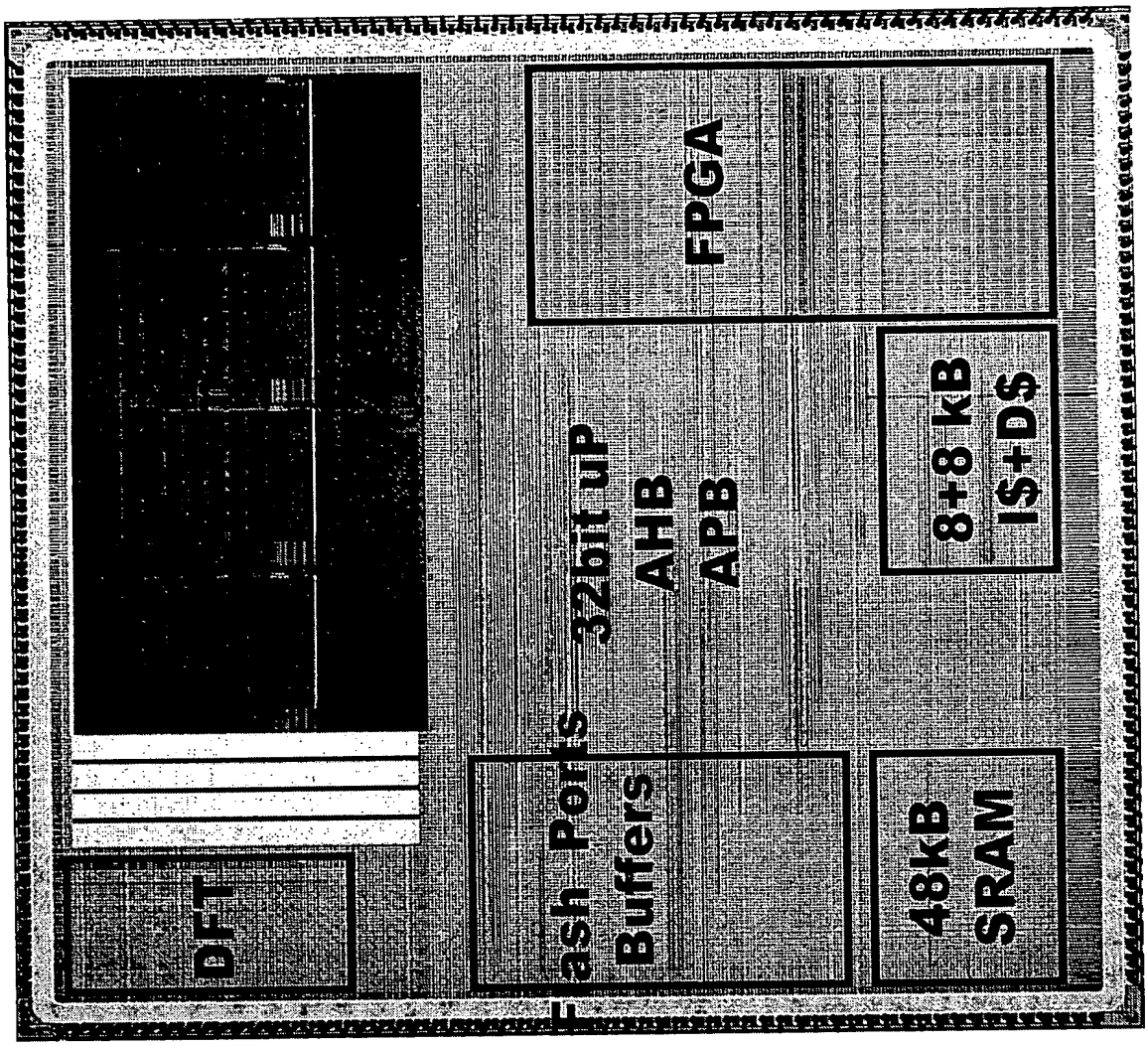
DFT
Flash Ports
Buffers
32bit uP
AHB
APB
FPGA
8+8 kB
I$+D$
48kB
SRAM

FIG. 7